NanoZeta Technologies is a world class provider of design, development, simulation, and measurement services for Analog, RF, Mixed Signal and Microwave components, subsystems and systems. The NanoZeta team combines a long standing experience and a unique combination of skills that has produced many successful and innovative designs.

Why NanoZeta ?

Meeting difficult RFIC performance specifications with cost effective silicon solutions that achieve short time-to-market are the primary advantages NanoZeta delivers to its clients. NanoZeta's extensive experience with proven designs, leveraged by its talented design team with numerous decades of cumulative Analog, RF and Systems Design experience, combine to make the NanoZeta team a top choice for high quality design of cost effective RFIC solutions.

With its talented team of engineers and close links to high quality academic institutions, NanoZeta is committed to the pioneering of technological advances in Analog and RF device modeling, circuit design and system architectures. NanoZeta continuously invests in IP development to remain in the vanguard of the next generation, high frequency wireless product suppliers.

Nanozeta's agile team and flexible structure, provides the customer with unique advantages. The customer can use the team as an extension of his internal team and allocate resources in an optimal way in order to achieve his schedule and budget objectives. In this manner, NanoZeta can provide cost effective Design Services through Virtual Private Network (VPN) to meet specific customer needs.

Standards

NanoZeta's design expertise of complex analog devices encompasses a broad range of IEEE standards, including:

- 802.11a/b/g/h/j WLAN (Wireless Local Area Network)
- 802.11n and higher speed enhancement for wireless video applications
- WiMAX (802.16d/e),the MWBA (Mobile Wireless Broadband Access) standard
- UWB (Ultra Wide Band) for high data rate medical and imaging applications
- WHDMI (Wireless High Definition Interface) for wireless imaging applications

IC Technologies

- TSMC Foundries nanometer processes
- Global Foundries nanometer processes
- ST Microelectronics Deep Submicron processes

Success Stories

NanoZeta's team has successfully completed Design, Simulation and Characterization of RF, Microwave and Millimeter Wave integrated circuits for 5GHz, 60GHz and 80 GHz tranceivers and sub-blocks (i.e. LNAs mixers, VCOs).

NanoZeta's team has successfully carried out the Design, Simulation and Characterization of Analog Integrated Circuits such as:

- Integer-N and Fractional-N PLLs
- Delay-Locked Loops (DLLs)
- Bandgap References
- Analog Front-Ends
- Analog Basebands

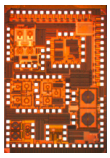
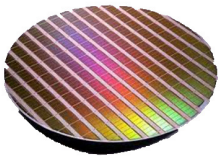
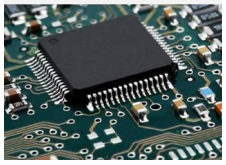
As well as subblocks such as:

- Programmable Variable Gain Amplifiers
- Filters
- Continuous Time Linear Equalizers (CTLEs)
- SSTL and LVDS High Speed IOs
- Operational Transconductance Amplifiers

NanoZeta's team has successfully completed Design, Development, Simulation and Characterization of Mixed Signal circuits for 5Gbit/s serial data communication interfaces such as:

- Equalizer - TX/RX
- DFE (Decision Feedback Equalizer)
- CML Output driver
- CML Buffer
- Latch
- MUX (Multiplexer Circuits)
- DFF (CML Based DFF)
- Phase Interpolator

NanoZeta's team has successfully completed in-lab projects for the measurement and characterization of analog, RF and microwave devices and systems.

NanoZeta Engineering team capabilities

	Education	Experience	Publicat'ns/ Patents	System Architecture	Digital Design	Analog Design	RF Design	Mixed Design	Analog/RF Layout	Project Managemnt
Sr. Tech. Advisor	BS Sc. Ph.D. EE	15 Yrs.	35/2	✓		✓	✓	✓	✓	✓
Senior Designer	BS Sc. MS EE Ph.D. EE	15 Yrs.	30/1			✓	✓	✓	✓	
Senior Designer	BS Sc. MS EE	8 Yrs.	4/0	✓	✓			✓		✓
Senior Designer	Dipl. Eng. MS EE	8 Yrs.	3/1			✓	✓		✓	
Senior Designer	BS Sc. MS EE Ph.D. EE	6 Yrs.	18			✓	✓		✓	
Mid.-Level Designer	BS Sc. MS EE	2 Yrs.	0/2			✓	✓		✓	
Jr.-Level Designer	BS Sc. MS EE	2 Yrs.	2/0			✓	✓		✓	
Project Manager	BS Sc. Ph.D. BA	25 Yrs.								✓

System Architecture

Transceiver
PLL/ Frequency Synthesizer
Analog Baseband
Analog Front End

Analog/Mixed Signal

Variable Gain Amplifiers
Linear-in-dB gain control
Voltage references
Fractional/Integer-N PLLs and sub-blocks
Analog Basebands
Analog Front-Ends

I.C. Technologies

down to 28nm, for CMOS/FDSOI
down to 0.13um, for BiCMOS

RF/MM-Wave

Low Noise Amplifiers
VCOs
Frequency doublers/quadruplers
Active and passive up/down conversion mixers
Fully Integrated 60-GHz transceivers
Fully Integrated E-band transceivers

Analog/RF Measurement Lab.

Test Plan Definition
Execution of Analog/RF measurements
Characterization in temperature and power supply
Data evaluation and presentation

NanoZeta Engineering team - Sampling of Experience

Senior AMS/RF IC Design Engineer

- **Education:** BSc in Physics, PhD in Electronics
- **Businesss Experience:** 15 years in Analog/RF/MS IC Design
- **Works and Publications:** Participated in projects developing a DDR2/3 PHY, a USB3 PHY, a 60GHz PLL, a great number of low jitter fractional-N/Integer PLLs, de-skewing PLLs and Spread Spectrum Clock generators. Full design flow of analog blocks (OpAmps, BGRs, CPs, VCOs, drivers) and RF Blocks (LNAs Mixers etc). Evaluating IC processes in 28fdsoi, 40nm, 65nm.

Author/coAuthor of 35+ pubblications in high level journals and conferences. Co-inventor of 2 patents.

Senior Analog/RF IC Design Engineer

- **Education:** BSc in Physics, MSc in Electronics, PhD in Electronics
- **Businesss Experience:** 15 years in Analog/RF/MS IC Design
- **Works and Publications:** Participated in projects developing a USB3 and a 60GHz PLL system. Design of high - speed parts, drivers, etc. Evaluating IC process in 65nm. Full design flow of analog blocks (OpAmps, BGRs, Sampling latches, Phase interpolator, drivers). Full design flow of CML high speed blocks and paths in transmitters/receivers. Design of integrated filters for broadband communication. Design of special high-speed (40Gb/s) electronic ICs for optical network applications (serializer part)

Author/co-author of 21 publications in high level journals and 9 conference papers. Co-inventor of 1 patent.

Senior Digital IC Design Engineer

- **Education:** BSc in Physics, MSc in Microelectronics
- **Businesss Experience:** 8+ years in Digital/Mixed signal IC Design
- **Works and Publications:** RTL design and verification of complex digital systems for CMOS imaging applications using a variety of EDA tools. Worked on several projects (cameras, photonic sensors, auto-focus devices) from specification to tape-out in cooperation with major customers. Design and verification of complex digital and mixed-signal ASICs (USB3.0 PHY, DDR2/3 PHY) using a variety of EDA tools. Responsibilities include system design/specification, full RTL-to-GDSII flow with sign-off verification at each step, semi-custom layout using signal integrity aware high-speed techniques,technical documentation.

Author or co-author of 2 publications in high level journals and 2 conference papers.

Senior Analog/RF Design Engineer

Education: Dipl.-Ing,.MSc in SoC Design

Businesss Experience: 8+ years in Analog/RF/MS IC Design

Works and Publications: Power Management Circuit Design and Verification focused mainly on Linear Dropout Regulators and DC-DC Buck converters for mobile phone applications. Free running oscillators, LVDS/SSTL drivers, Continuous Time Linear Equalizers

Author or co-author of 2 publications in high level journals and 1 conference paper. Co-inventor of 1 patent.

Senior Analog/RF Design Engineer

- **Education:** BSc in Physics, MSc in Electronics, PhD in Electronics
- **Businesss Experience:** 6+ years in Analog/RF/MS IC Design
- **Works and Publications:** Bandgap Reference, temperature sensor, class-AB amplifier, buck converter power stage, evaluation/characterization of devices for switching applications. Mixed-signal circuits for power management applications (series linearregulator, POR, Switched-Cap blocks, comparators, OTAs). Mixed-signal circuits for 5Gb/s serial data communication interfaces(Equalizer-TX/RX, DFE, CML Output Driver, CML Buffer, Latch, MUX,DFF, Phase Interpolator). Digital-assisted DC offset cancellation loop. Fully-balanced OTA-C 7th-order 100MHz Elliptic lowpass filter for Powerline AFE. 300MHz, 60dB-linear PGA with 1.4dB step for Powerline AFE

Author/Co-author of 18 papers in refereed international journals and conferences.

Mid-level Analog IC Design Engineer

- **Education:** BSc in Physics, MSc in Electronics
- **Businesss Experience:** 4+ years in Analog/RF/MS IC Design
- **Works and Publications:** Analog/RF IC and physical design using EDA tools. Electrical Design, Physical Design and Verification of a USB2.0 UTMI transceiver. Design of a wideband (65MHz to 3GHz) LNA for ITU-T G.hn (G.9960 and G.9964) applications with variable gain, low noise figure and high linearity. Design of a 1GHz Low-Voltage Differential Signaling driver/receiver. Design a 6-bit flash ADC at 1.7, 2.5, and 5GHz sampling rates, implementaing in 1.2V using a new offset calibration technique.

Author or co-author of 2 conference papers.

The NanoZeta Management

Summary

The NanoZeta Tech management is simple in structure, exceedingly efficient and provides the customer with an extensive array of Experiences in all facets of Semiconductor design and development with a distinct Customer orientation

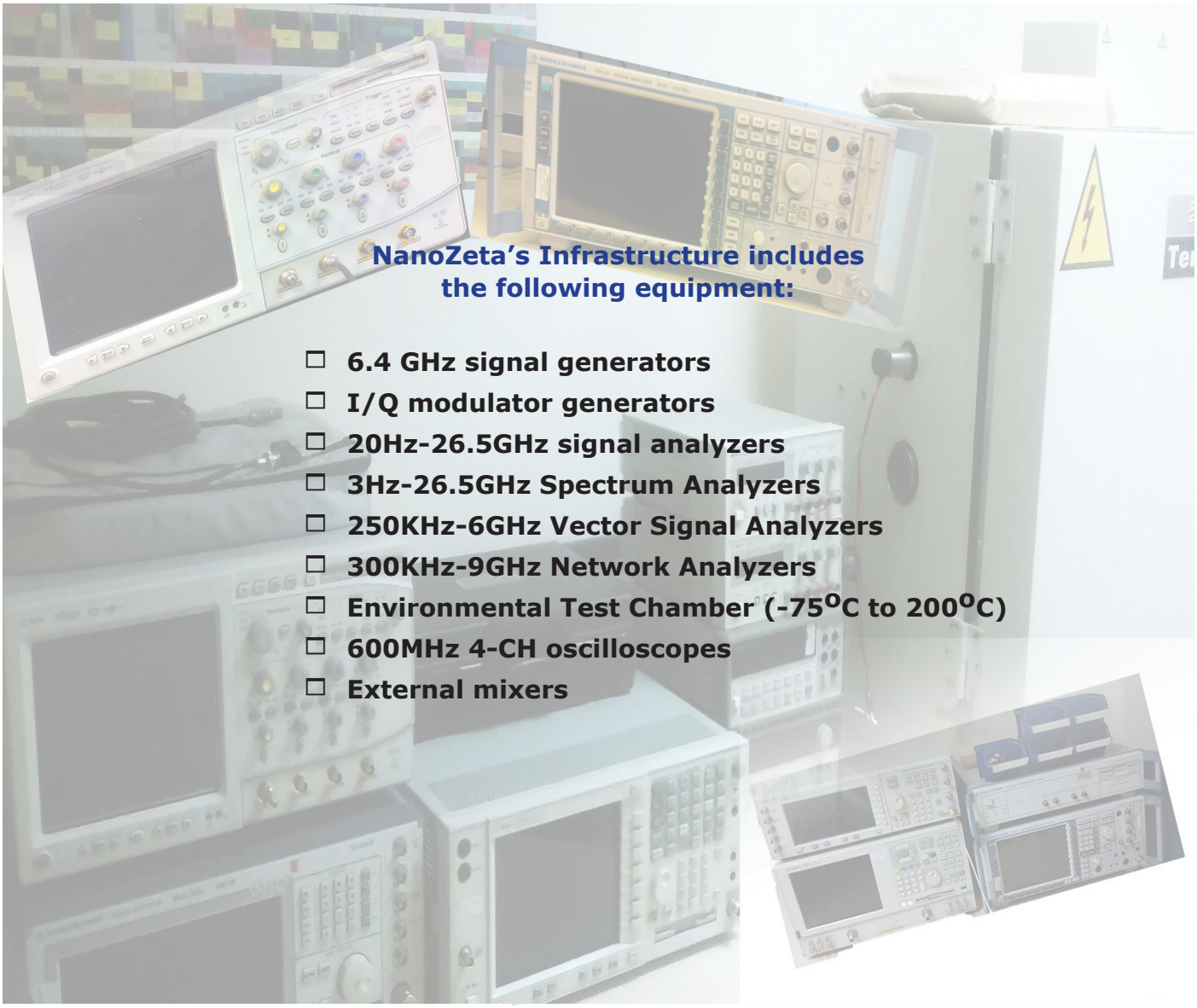
Mikes Sisois Ph.D., General Manager

Dr. Sisois has been President of Theta Microelectronics, Inc. and Managing Director of Theta SA, for the period March 2010-March 2015. He directed all operations of this advanced design group that developed and built leading edge semiconductor designs in the wireless Point-to-Point communications space.
Dr. Sisois was part of the original team that started Atmel Corporation in 1984. Over time, Atmel became a leader in the design and manufacture of microcontrollers, advanced logic, mixed-signal, nonvolatile memory and radio frequency (RF) semiconductor components. As the fourth Atmel employee, Dr. Sisois spent over 20 years in senior management positions with that company. As the CIO and V.P. of Strategic Planning, he managed the business planning process of the enterprise, coordinating the activities of dozens of engineering groups, a global field sales force in over 30 countries, a number of marketing groups and a supply chain of internal manufacturing facilities and external partners around the globe.
Prior to this, Dr. Sisois was employed by Seeq Technology in . He came to Seeq from the University of Santa Clara where he was a faculty member and responsible for the information systems infrastructure of the University. After leaving Atmel in 2006, Dr Sisois rejoined the faculty of the University of Santa Clara. He also served as a senior management consultant with SAP , in their Palo Alto Labs.
He holds a B.S. In Computer Engineering from California State University at San Jose, California. He also holds both an MBA and a Ph.D. from the University of Santa Clara, California.

Fotis Plessas, Ph.D., Chief Technology Officer

Dr. Plessas is an Analog/Mixed Signal and RF Design Engineer. He is working or has worked under contracts with the Industrial Systems Institute (ISI/Athena RC), the Institute of Communications and Computer Systems (ICCS/NTUA), Analogies S.A., Theta Microelectronics, HDL-DH, Nanozeta Technologies and through subcontracting with larger US, European, and Middle East Firms (more information can be provided under NDA). From 2007 to 2013, he was with Analogies S.A, as a Senior Engineer and Manager responsible for the development of high-speed wired and wireless connectivity cores for SoC solutions (i.e. a USB3.0 PHY, a DDR2/3 PHY and a 60GHz PLL). Prior to Analogies he was involved in several research activities at the Applied Electronics Laboratory and the Industrial Systems Institute working mainly in the area of RF communication circuits and analog and mixed-mode circuit design. His research interests focus on the design, analysis and implementation of Analog, RF and millimeter-wave circuits, PLL- and injection-locking- based frequency synthesizers. He has extensive experience in wired and wireless communication systems engineering and he is the author or co-author of more than 34 journal and conference papers. Dr. Plessas is a member of IEEE, and IEEE MTT/CAS/SSC societies. He received his Ph.D. in Electrical Engineering from Patras University, Greece. He holds an MBA and a B.S. degree in Physics from the same university. His professional experience includes 15+ years in Engineering/Technical Management and 3+ years in consulting.

NanoZeta Infrastructure and Facilities



NanoZeta's Infrastructure includes the following equipment:

- ☐ 6.4 GHz signal generators
- ☐ I/Q modulator generators
- ☐ 20Hz-26.5GHz signal analyzers
- ☐ 3Hz-26.5GHz Spectrum Analyzers
- ☐ 250KHz-6GHz Vector Signal Analyzers
- ☐ 300KHz-9GHz Network Analyzers
- ☐ Environmental Test Chamber (-75^{O}C to 200^{O}C)
- ☐ 600MHz 4-CH oscilloscopes
- ☐ External mixers

Nanozeta makes available to the customer Services and Test Equipment dedicated to providing quick and reliable measurements that can be geared to specific customer needs

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