SILICON-PROVEN DESIGN HIGHLIGHTS

Selected PLL, TRANSCEIVER and RF designs

NanoZeta Tech

NanoZeta delivers silicon-proven PLL, RF/mmWave, and mixed-signal ICs from 130 nm to 5 nm. Below are selected designs* demonstrating our capability across low-power IoT, high-performance frequency synthesis, and mmWave radar.

OUR APPROACH

Early modeling, architecture-to-layout co-design and tight simulation-to-silicon correlation on first silicon

Low-Power Integer-N PLL 2.45 GHz

Process: 130 nm TSMC
Application: IoT BLE

Challenge:

- Achieve <1.5 mW at 1 V in a 130 nm, 2.45 GHz BLE PLL; support 4 kHz-step direct DCO GFSK modulation.

Approach:

- Low-voltage biasing and current minimization across all PLL blocks.
- VCO capacitor-bank architecture with ~100 aF step; iterative layout tuning for linearity.

Result:

- <1.5 mW operation over corners; VCO phase noise −113 dBc/Hz @ 1 MHz.
- ~100 aF DCO step with linearity meeting BLE modulation requirements.

Fractional-N PLL 17–20 GHz

Process: 5 nm TSMC
Application: Optical SerDes

Challenge:

- <200 fs RMS jitter at 37.5 GHz in 5 nm; maintain RF performance under extreme FinFET variation.

Approach:

- Low-noise loop with controlled reference, quantization, and CP noise.
- VCO architecture and device selection optimized for 5 nm sensitivity.
- Layout refined to reduce parasitics in critical RF paths.

Result:

- <200 fs jitter achieved across PVT; VCO FOM ~182 dB with full corner coverage.

*Performance values shown are representative; customer NDAs apply.

www.nanozetatech.com | athens@nanozetatech.com

From architecture to silicon-proven ICs — precision analog, RF & mixed-signal design

NanoZeta Tech

SILICON-PROVEN DESIGN HIGHLIGHTS

Fractional-N PLL 7–10 GHz

Process: 22 nm FDSOI GF
Application: Automotive Radar

Challenge:

- Meet automotive radar phase-noise specs from 100 kHz–10 MHz offset under tight on-chip integration and layout constraints.

Approach:

- Bias VCO and charge pump for minimum phase noise without FOM loss. Use fully EM-extracted VCO layout (inductor and upper-metal routing) tuned to control parasitics.

Result:

- PLL meets spec over PVT; −116 dBc/Hz @ 1 MHz offset (3.5 MHz BW, including reference noise).
- VCO FOM ~190 dB and −140 dBc/Hz @ 10 MHz offset.

57–64/66 GHz Radar-on-Chip

Process: 65 nm TSMC
Application: Industrial Radar

Challenge:

- Implement a full radar transceiver-on-chip (8×Rx, 2×Tx, analog baseband, on-chip PLL).
- Maintain amplitude and phase control across a 60 GHz LO network spanning the die.

Approach:

- Co-design of Rx, Tx, baseband, and PLL with system-level performance as target.
- Full EM-extracted 60 GHz LO distribution (passives + transmission lines) optimized for loss and phase.

Result:

- Silicon-verified radar-on-chip with ~9 GHz chirp, Tx linearity on-spec, and LO phase noise meeting radar FOM.

Timing and Frequency Solutions (mass-production-proven)

- 96 MHz; 24.576–384 MHz; 480 MHz; 20 GHz Integer-N PLLs
- 528 MHz and 13.5–16.5 GHz Fractional-N PLLs

RF/mmWave (silicon-proven)

- 76–81 GHz Rx-RFFE and analog baseband; LNAs and mixers up to 80 GHz
- 57–66 GHz linear PA; 2.45 GHz switched-mode PA

RF, Analog & Mixed-Signal Subsystems

- Op-amps, level shifters, temperature sensors, SPI, BGRs, LDOs (production-proven)
- 14-bit SAR ADC, 2 MS/s (silicon-proven)

www.nanozetatech.com
athens@nanozetatech.com

CYPRUS
GREECE
ISRAEL
USA